Remarks/Arguments

The Office Action mailed October 3, 2007 has been reviewed and carefully considered.

Claims 1 and 7 have been amended. Claims 1-12 remain pending in this application.

Reconsideration of the above-identified application, as herein amended and in view of the following remarks, is respectfully requested.

Claim objections:

Claims 1-12 stand objected to for informalities. Specifically, the use capitalized term "Read Address" has been objected to. Throughout the specification as originally filed, each instance of "Read Address" is shown with the two words capitalized. As such, the claims are simply using the same term as recited by the specification. The use of capital letters is not prohibited and in this case clearly tracks the use of the term in the specification. Reconsideration and withdrawal of the rejection is respectfully requested.

In addition, the Examiner states that claims 1 and 7 recite "within one a prescribed threshold", which appears to be missing words." A review of claims 1 and 7 do not show such recitation as asserted by the Examiner. Each claim recites "...to maintain capacity below a prescribed threshold." Applicant does not see any problem with this language as originally presented, and kindly requests reconsideration of the objection by the Examiner.

Claim rejections

Claims 1-12 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite. More specifically, the user of the language "on the order of" f_n, has been objected to as being indefinite. Claims 1 and 7 have been amended to clarify the intended claim language. Particularly, the claims have been amended to clarify that the application of successive read addresses to the memory is performed at a rate slower than and related to the frequency rate (fn) of said applying successive read clock pulses... As can be seen from the specification at page 4, lines 23-26, the address generator applies the read addresses to the FIFO at a slower rate than the received read clock pulse rate, but is still on the order of f_n, such that the amended claim language clarifies this aspect of the present principles. Reconsideration and withdrawal of the rejection is respectfully requested.

Claims 1, 6, 7 and 12 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,805,198 to Stern et al. In asserting this rejection, the Examiner has cited Stern et al. at Col. 3, line 11 – Col. 4, line 12, and Figure 1 showing a 4X output of the oscillator. Unfortunately, this does not anticipate, nor even render obvious the claimed principles as set forth in independent claim 1 and 7.

Claim 1 states, *inter alia*, "applying successive read clock pulses to the memory at a frequency of xfn...." and "applying successive read addresses to the memory at a rate slower than xf_n..."

According to Stern et al., incoming data is clocked into the FIFO at a rate set by the incoming or external clock and is clocked out of the FIFO by the clock signal derived from an internal tunable crystal oscillator. A digital timing or phase comparison circuit monitors the relative timing relationship between the incoming clock and the oscillator generated internal clock and provides signals to the oscillator to vary the frequency of the oscillator as necessary to keep the FIFO half full of data, on the average. (See Col. 3, lines 17-26). In reviewing the remainder of the disclosure, applicant cannot find any language in Stern et al. that discloses or suggests applicant claimed *applying successive read addresses to the memory at a rate slower than xf_n at which the read clock pulses are applied.* In fact, Stern et al. teaches away from this concept by using a comparison to determine which FIFO register is being addressed by the external clock signal on line 16 at a time when the divide by 4 signal on line 32 is switching from addressing the 8th cell to addressing the 9th cell. Thus, there is no indication that the application of successive read addresses to the memory is performed at a rate slower than the rate at which the read addresses are applied to the FIFO. Reconsideration and withdrawal of the rejection is respectfully requested.

Regarding claims 6 and 12, Stern et al. does not disclose or suggest applying successive read clock pulses to the memory at a frequency 4 times the frequency f_n. In fact, Stern et al. teaches the generation of a 4X clock signal from the oscillator that is input into synchronization circuits 135-137 shown in Figure 3A. The divider 30 makes sure that the 4x clock signal is divided by 4 before it is provided to the memory (FIFO). Thus, there is no teaching by Stern et al. that the read clock pulses are applied to the *memory (FIFO)* at a frequency that is 4 times that of the initial frequency. In fact, it could be argued that Stern et al. actually teaches away from this concept by showing the generation of the 4X clock signal, applying it to other external synchronization circuits and not the FIFO, and dividing it by 4 before applying it to the FIFO. Reconsideration and withdrawal of the rejection is respectfully requested.

Claims 2-5 and 8-11 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Stern et al. in view of U.S. 2007/0116062 to Spalilnk. Claims 2-5 and 8-11 depend from claims 1 and 7, respectively. The Spalilnk does not overcome the deficiencies of the Stern et al. patent, and thus, the combination of these two patents would not render obvious independent claims 1 and 7, claims 2-5 and 8-11 that depend therefrom. Reconsideration and withdrawal of the 35 U.S.C. 103(a) rejection of claims 2-5 and 8-11 is respectfully requested.

Conclusion

In view of the foregoing amendments to the claims and the accompany remarks, applicants solicit entry of this amendment and allowance of the claims. If, however, the Examiner believes such action cannot be taken, the Examiner is invited to contact the applicant's attorney at (609) 734-6820, so that a mutually convenient date and time for a telephonic interview may be scheduled.

Kindly charge any additional costs, or credit any refunds to Deposit Account **07-0832.**

Respectfully submitted,

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